

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yukio NISHIDA, et al.

SERIAL NO: 10/623,563

GAU:

FILED: July 22, 2003

EXAMINER:

FOR: MANUFACTURING METHOD FOR A SEMICONDUCTOR DEVICE

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

**REFERENCES**

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**RELATED CASES**

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**CERTIFICATION**


- ☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

**DEPOSIT ACCOUNT**

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Form PTO 1449  
(Modified)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTACHMENT NO.

240547US2

SERIAL NO.

10/623,563

## LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Yukio NISHIDA, et al.

FILING DATE

July 22, 2003

GROUP

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	2002/0100945 A1	08/01/2002	J. A. MANDELMAN, et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AO	2002-222947	08/09/2002	JAPAN (with English extract)		X
	AP	2002-305287	10/18/2002	JAPAN (with corr. US 2002/1011945 A1)		X
	AQ	9-82958	03/28/97	JAPAN (with English extract)		X
	AR					
	AS					
	AT					
	AU					
	AV					

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	T. GHANI, et al., IEDM Technical Digest, pages 415-418, "100 NM GATE LENGTH HIGH PERFORMANCE / LOW POWER CMOS TRANSISTOR STRUCTURE", 1999				
	AX	T. MATSUMOTO, et al., IEDM Technical Digest, pages 219-222, "70 NM SOI-CMOS OF 135 GHz $f_{\max}$ WITH DUAL OFFSET-IMPLANTED SOURCE-DRAIN EXTENSION STRUCTURE FOR RF/ANALOG AND LOGIC APPLICATIONS", 2001				
	AY	K. OTA, et al., Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, pages 148-149, "80 NM HIGH PERFORMANCE CMOSFET WITH LOW GATE LEAKAGE CURRENT USING CONVENTIONAL THIN GATE NITRIC OXIDE", 2001				
	AZ				<input type="checkbox"/> Additional References sheet(s) attached	

Examiner

Date Considered

\*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.